Amendments to the Specification

Please replace the paragraph beginning on page 8 at line 8 with the following:

A hardware implementation for providing initial OFDM clock synchronization using the above method is shown in Figure 2. A receiver component 20 is shown which is the portion of the receiver that is relevant to clock synchronization. The digitized, received data enters at the input and is presented to both the N-point cross correlator 24 and the vectorizer 26. The vectorizer 26 is preferably a large serial-to-parallel shift register. Data is serially shifted into the vectorizer 26, while data is taken out in blocks of 64. (Note that the data paths are complex implying real and imaginary parts known as the I and Q signals in our case.)